REMARKS

Claims 1-4 and 6-40 are pending in the application, of which claims 3, 4, 6-27, 29-32, 34, 35, 37 and 38 have been withdrawn from consideration. By this Amendment, claim 1 has been amended and claims 33 and 36 have been cancelled. No new matter has been added. It is respectfully submitted that this Amendment is fully responsive to the Office Action dated October 5, 2007.

Allowable Claimed Subject Matter:

Applicant gratefully acknowledges the indication in item 8 of the Action that claim 40 has been allowed.

Applicant also gratefully acknowledges the indication in item 7 of the Action that claim 2 would be allowable if rewritten in independent form to include all of the features of its base and intervening claims. However, for at least the features set forth below, it is respectfully submitted that all of claims 1, 2, 28 and 39 are allowable.

Claim Objections:

The Examiner states that "in photoelectric converter and the first transistor being adjacent to each other in the row direction" in claim 1 should be corrected to read as – wherein the photoelectric converter and the first transistor being adjacent to each other in the row direction--.

Accordingly, "in photoelectric converter" in claim 1 has been changed to read "in the photoelectric converter". Thus, the claim objection should be withdrawn.

Claim Rejections under 35 U.S.C. §112, §101 and §102

Claims 33 and 36 stand rejected under 35 U.S.C. §112, §101 and §102. Inasmuch as claims 33 and 36 have been cancelled, the claim rejections are moot and must be withdrawn.

Claim Rejections under 35 U.S.C. §103

Claims 1, 28 and 39 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Koizumi* (USP 7,081,607) in view of *Guidash et al.* (USP 6,466,266). This rejection is respectfully traversed.

It is submitted that the language "the gate electrode of the first transistor and the gate electrode of the fourth transistor being extended in the column direction" in claim 1 has been changed to –the gate electrode of the first transistor and the gate electrode of the fourth transistor being arranged so that a gate width direction thereof corresponds to the column direction--.

As shown in, e.g., FIG. 9 of the present application, the gate electrode of the first transistor (28_{TG}) and the gate electrode of the fourth transistor (28_{SEL}) are arranged so that a gate width direction thereof corresponds to the column direction. Additionally, in the specification of

the present application, the extending direction of the gate electrode is defined by the column direction or the row direction and the gate width direction. For example, it is described in, e.g., page 41, line 25 ~ page 42, line 1, that all the gate electrodes are extended in the row direction, i.e., with the gate width extended in the row direction. It is also described in, e.g., page 88, lines 6-8 that all the gate electrodes are extended in the column direction, i.e., with the gate width extended in the column direction. Thus, it is submitted that the amendments to claim 1 do not raise the issue of new matter.

As described in claim 1, the claimed invention has features that in each pairs of the pixel units of the n^{th} row and the $n+1^{th}$ row corresponding to each other, the gate electrode of the first transistor of the pixel unit of the n^{th} row and the gate electrode of the fourth transistor of the pixel unit of the $n+1^{th}$ row are formed in one continuous pattern of a same conducting layer, and the gate electrode of the first transistor and the gate electrode of the fourth transistor are arranged so that a gate width direction thereof corresponds to the column direction. The gate width is defined by the width of the active region where the gate electrode formed thereabove. The width of the active region is defined by the device isolation film. The terms: "gate width" and "gate width direction" are technical terms widely used in the technical field of the semiconductor devices.

The Examiner states that although *Koizumi* does not teach that one continuous pattern forming the gate electrode of the first transistor of the pixel unit of the n^{th} row and the gate

electrode of the fourth transistor of the pixel unit of the $n+1^{th}$ row are formed of a same conducting layer, and the gate electrode of the first transistor and the gate electrode of the fourth transistor are extended in the column direction, *Guidash et al.* teaches in FIG. 4 that a gate of a transistor of one row and a gate of another transistor of an adjacent row are continuously formed within a same conducting layer, and the gate electrode 21 of the first transistor and the gate electrode RSG of the fourth transistor are extended in the column direction.

However, in *Guidash et al.*, although the gate electrode of the first transistor (TG) of one row and the gate electrode of the third transistor (RG) of adjacent row are formed in one continuous pattern of a same conducting layer, the gate electrode of the first transistor (TG) of one row and the gate electrode of the fourth transistor (RSG) of adjacent row are not formed in one continuous pattern of a same conducting layer. *Guidash et al.* neither teaches nor suggests that the gate electrode of the first transistor (TG) of one row and the gate electrode of the fourth transistor (RSG) of adjacent row are formed in one continuous pattern of a same conducting layer.

In *Guidash et al.*, the gate electrode of the first transistor (TG) is arranged so that a gate width direction thereof corresponds to the row direction, and the gate electrode of the fourth transistor (RSG) is arranged so that a gate width direction thereof corresponds to the column direction (see FIG. 4). *Guidash et al.* neither teaches nor suggests that both of the gate electrode

of the first transistor (TG) and the gate electrode of the fourth transistor (RSG) are arranged so that a gate width direction thereof corresponds to the column direction.

As described above, *Guidash et al.* is clearly different from the present invention and does not provide any motivations for the present invention. Thus, the present invention would have been unobvious to one of ordinary skill in the art, even if both of *Koizumi* and *Guidash et al.* are considered.

In view of the aforementioned amendments and accompanying remarks, Applicant submits that that the claims, as herein amended, are in condition for allowance. Applicant requests such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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